

Notice of References Cited		Application/Control No. 10/816,791	Applicant(s)/Patent Under Reexamination MACCHETTI ET AL.	
		Examiner Martin Jeriko P. San Juan	Art Unit 2109	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,243,470 B1	06-2001	Coppersmith et al.	380/259
*	B	US-5,710,731	01-1998	Ciraula et al.	708/706
	C	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Morioka et al. "An Optimized S-Box Circuit Architecture for Low Power AES Design, Cryptographic Hardware and Embedded Systems - Ches 2002. 4th International Workshop Revised Papers (Lecture Notes in Computer Science Vol 2523), Pages 172-186, XP002254730
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.